Next Generation Silicon Sub-cells for High Efficiency III-V/Si Multi-junction Solar Cells

Project results and lessons learnt

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Executive Summary

During the first 18 months of this project the target was to determine the viability of a novel design of III-V semiconductor materials on silicon multi-junction solar cell. The III-V on silicon multi-junction approach offers the prospect of high efficiency with lowered costs due to the use of industrially ubiquitous silicon. Working closely with our collaborators at Ohio State University in the United States, we have worked on developing alternative structures to achieve these ends. During this period our collaboration has achieved the world record efficiency for a two junction multi-junction III-V on silicon device, providing proof of the leading role this team is playing.

Work has covered the use of more conventional structures for the silicon bottom cell, with UNSWs deep knowledge in silicon processing being used to explore different rear structures to achieve highest performance. Utilisation of a room temperature metal contacting technique developed in another ARENA funded project has begun, an approach expected to provide benefits due to the lack of high temperature processing required. Detailed simulations have also been performed, using an advanced device simulator tool, TCAD, to explore the use of alternate materials for the rear surface of the silicon cell. Materials that will preferentially block electron flow at the rear have been identified and are currently being explored for use in advanced designs.

Reduction of silicon used in these devices is being explored by the use of silicon thinner than previous efforts. The challenges of using this approach remain substantial, but encouraging results suggest this is a worthwhile approach. All of the technical milestones for this reporting period have been met, with further deep improvements to come. The ultimate goal of looking at completely new designs for III-V on silicon solar cells remains viable for this project.

Project Overview

Project summary

In the first eighteen months of this project the work has focused on developing a method for ensuring the material quality for both n and p type silicon is maintained during the gallium phosphide/gallium arsenide phosphide (III-V) deposition process. The minority carrier lifetime is a key parameter for silicon solar cells, setting hard upper limits on the performance of completed devices. Previous research by our team, as well as other international teams, saw a deep degradation of silicon minority carrier lifetime when the III-V deposition was completed. Through an exhaustive experimental effort and drawing on key knowledge and expertise at UNSW, we have determined two causes for this degradation and have developed an approach to avoid this potentially disastrous effect during fabrication. The results of our efforts are to be reported on in the IEEE run technical conference for PV specialists. The resolution of this issue opens up the way for rapid improvements in III-V on silicon multijunction device performance.

At the same time a simulation model has been completed using the Sentaurus Technology Computer-Aided Design (TCAD) platform to assess the impact of III-V growth on the silicon solar cell, in terms of the modifications to the front of the silicon cell. Detailed characterisation of fabricated structures has allowed us to determine the key properties of the interface between the III-V material and the silicon, allowing for improved designs. As well, the inclusion of so-called carrier selective contact materials has also been achieved, along with more conventional amorphous silicon, for use on the rear surface of the silicon cell. Combined with encouraging early results, two metal oxides, nickel oxide and vanadium oxide, have been identified as being of interest for incorporation into a final novel structure. A working device using nickel oxide as a carrier selective contact has been demonstrated, with further refinements expected to rapidly improve the performance of these devices.

The carrier selective contact type of approach should allow for thinner silicon substrates to be used, reducing material usage and delivering further cost reductions to the solar cell fabrication process. Work has already begun on the use of thinner silicon substrates. The results have shown that management of the strain build up in the full structure will be an important parameter to control during the fabrication. High quality material has been found to be possible, there are, however, downstream issues to resolve to produce a greater yield of devices due to bowing of the substrates. This work will continue.

The incorporation of a room temperature metal contacting technique, that uses electric breakdown of an insulating layer on the rear of the silicon has also been applied to III-V on silicon devices. A working device has been delivered, but there remain challenges to create high performance devices, mainly due to unrelated processing issues that will require ongoing effort to resolve, but pose no fundamental barrier to achieving the outcomes aimed for in this project. With the improvements to our process flow delivering better final silicon performance we have every confidence these results will improve rapidly.

Project scope

This project seeks to develop a III-V on silicon multi-junction solar cell device with the goal of the fabrication being compatible with industry. The III-V on silicon approach combines the high performance of III-V materials (these are the basis for the highest efficiency devices existing today) with the cost and industry expertise of silicon. The aim is to deliver both lowered cost and high performance.

The problem for multi-junction solar cells in general is the high cost, due to the use of germanium substrates and relatively expensive fabrication techniques for the III-V material deposition. Previously the integration of III-V material with silicon had proven extremely challenging, but in recent years the use of offcut substrates and insights into the initial growth of III-V on silicon has enabled the growth of III-V based solar cells on silicon. The development of a high performance silicon solar cell in the silicon substrate has proven more challenging than first realised with initial results indicating severe reductions in performance for the silicon after undergoing III-V deposition.

This project has built on earlier work [1] to overcome this issue, developing a number of strategies to preserve the silicon minority carrier lifetime (the key determinant of potential performance for the silicon cell). The exact nature of the causes of this effect is still being resolved, but the protection of the silicon has been proven, enabling the achievement of much higher performance. Work is ongoing to provide lifetime protection in a manner that reduces process complications, with significant effort expected on this task in the next 12 months.

The overall goal of this project is to enable a novel approach to III-V on silicon using thinner silicon substrates, to reduce material usage, and to simplify processing by including a heterojunction type rear surface. Growth of III-V on these thinner substrates needs to be optimised and the processing of the structures will need to be refined. This project aims to develop the knowledge and expertise to achieve a high performance multi-junction device on silicon, with reduced cost compared to conventional multi-junction devices and with reduced material usage.

Outcomes

During the initial period of the project the main issue was the baffling degrading nature of the silicon minority carrier lifetime. Since this provided a major impediment to high performance silicon solar cells a great deal of the effort has been directed to solving this issue. Processes for preventing the degradation have been developed in the time period, the exact nature of the process itself still needs to be fully resolved. It is intended to study this in more detail in the subsequent periods of the project to try and identify potentially simpler methods for lifetime protection.

We also looked at the problem of light trapping for our devices. This will be critical for thinner silicon substrate devices due to the relatively poor light absorption of silicon. Texturing of the silicon surfaces is standard in commercial solar cells today, but this approach is not immediately compatible with the

[1] "On the Origin of Silicon Lifetime Degradation During Anneal in III-V Material Growth Chambers," C. Yi, N. Western, F. Ma, A. Ho-Baillie, S. Bremner, presented at the 46th IEEE Photovoltaic Specialist Conference, Chicago, June 2019.

structures which we are fabricating. To this end we have explored the use of rear texturing for the silicon solar cell and also an additive layer to enhance light trapping in the silicon in particular. The additive layer was not originally planned, but offers advantages in that the thickness of the III-V device may also be reduced due to the enhanced light path length in the device. Encouraging results have been found and we intend to explore this solution further as this project moves forward.

The minority carrier lifetime degradation is a key barrier to implementing a commercially relevant III- V on silicon device. The solution of this is a major breakthrough for our project and it is anticipated that performances of final devices can now be increased significantly from previous efforts. This is highly encouraging as the previous efforts by the UNSW and OSU teams saw the establishment of a world record efficiency for a two junction device. The initial results for simplified processing that can accompany the heterojunction rear approach for silicon can also be leveraged to deliver a final outcome relevant to industry.

All of the technical milestones for the first reporting period have been met. There is great scope for improvement of the performance for some of the approaches, but these are early days and many of the performance issues will now be rectified due to the lack of silicon performance degradation. Improvements are expected to be rapid once key equipment is installed at UNSW and brought back online at OSU.

An unexpected highlight for the project was the improvement of performance using an additive textured Polydimethylsiloxane (PDMS) layer to improve performance. This was used with our monolithic devices and results indicate a significant improvement in performance. We intend to pursue this approach as the project proceeds.

Transferability

The development of robust silicon preservation process is to be reported to the PV community in the very near future at the leading technical conference for PV. This will offer researchers a method for ensuring the silicon performance is not impacted by the III-V deposition step and allow for high performance silicon cells in the multi-junction devices. This should enable rapid improvements in performance of devices translating to rapid increases in record performances reported. The PDMS additive layer results have also been reported, showing a relatively straightforward way to improve performance. It is applicable to many different structures beyond our layout.

Conclusion and next steps

In conclusion, this project has been able to achieve all of its technical milestones. The importance of these milestones is that achieving them indicates the feasibility of the approaches being undertaken. The use of nickel oxide to create a rear structure for the silicon in a III-V structure is a key step, with processing issues overcome to deliver a device that provides a proof of concept. While the performance is relatively modest, we have already identified ways to significantly improve performance through some simple modifications that have already been developed here at UNSW. The fabrication of a thin silicon based device has proven a challenge due to the processing issues brought about by the flexibility of the silicon when the thickness is below 200 microns. Obtaining a working device is a significant breakthrough in this effort. Incorporation of a patented room temperature metal contacting technique with a III-V on silicon structure has proven

challenging, with handling procedures for the structures requiring refinements. Again, a modest performance is expected to be rectified quickly, as the issues limiting their performance have been identified and are currently being rectified.

The next steps for this project are significantly increasing the efforts in metal oxide layers at the silicon rear. This will be enabled by the acquisition of an advanced atomic layer deposition tool to give excellent control over the oxide properties. Combined with our improved processes for protecting silicon performance, we expect to see rapid improvements in performance over the next six months. This will align our outcomes to the stated goals of the project.

Lessons Learnt

Lessons Learnt Report: Silicon minority carrier lifetime degradation

Project Name: *Next Generation Silicon sub-cells for high efficiency III-V/Si multi-junction solar cells*

Knowledge Category:	Technical
Knowledge Type:	Technology
Technology Type:	Solar PV
State/Territory:	NSW/USA

Key learning

The silicon minority carrier lifetime problem was already known prior to commencing the project, what we learnt is that the real reasons for seemingly conflicting reports on the nature of the problem have a surprisingly straightforward explanation.

Implications for future projects

Any project where silicon is subjected to high temperatures is potentially impacted by our findings.

Knowledge gap

What was noticed was that some groups reported remedies for the silicon minority carrier lifetime problem, but that other groups found these approaches did not help. We also observed that procedures reported elsewhere as preserving lifetime were ineffective. We decided there must be something else going on that explained the seeming contradictions in the literature.

Background

Objectives or project requirements

We needed a robust procedure to ensure lifetime remained unaffected during III-V deposition. It was therefore necessary to explore what processes caused this degradation and what approaches might work to prevent it.

Process undertaken

We leveraged the presence of a III-V deposition tool at UNSW to conduct our own experiments. We also sent silicon substrates to other facilities to check what was observed for the same processes.

The presence of contaminants in the silicon is implied for the lifetime degradation, so attempts were made to identify the identities of the contaminants. Due to the very low concentrations involved this proved exceedingly difficult to achieve, but several potential contaminants were identified. These corresponded with reports from other groups. We then used the exact same procedure as employed in a report that suggested silicon nitride layers on the rear of the silicon prevents contamination during III-V processing. We still observed a degradation. Consulting with our colleagues at UNSW looking at the problem of light and temperature induced degradation of silicon solar cells, and consulting the literature in that research area, we investigated the impact of different annealing temperatures on the silicon substrates. Our results showed unambiguously that the presence of grown-in defects could also catastrophically degrade silicon performance. This led us to the conclusion that the degradation is due to two reasons, grown-in defect activation from simply heating the substrate, plus contamination in the deposition chamber.

Shown in the supporting information are key results we used to identify the grown-in defect activation explanation.

The solution is a high temperature anneal before processing starts, plus the use of a silicon nitride layer on the rear of the silicon prior to III-V deposition. This does complicate the process flow somewhat, so we are looking at methods that will achieve the same outcome without unnecessarily complicating the process flow.

Supporting information (optional)

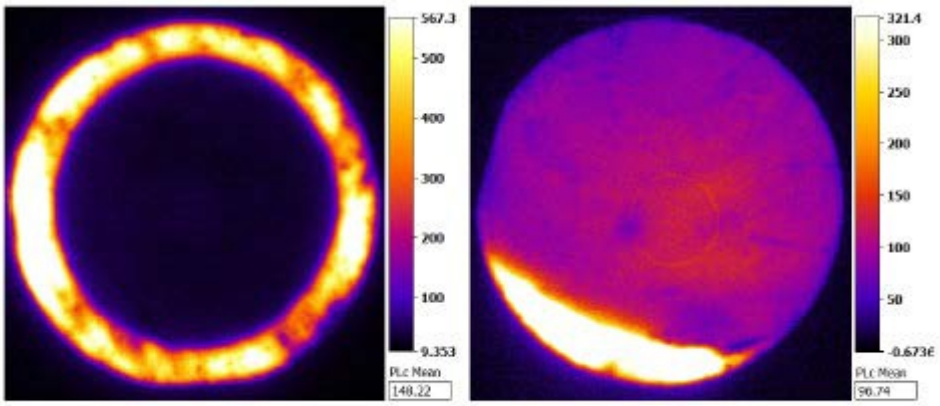

Figure 1: Photoluminescence images of n type (image (a)) and p type (image(b)) silicon wafers furnace annealed at 550 °C. The dramatic drop in lifetime is indicative of the activation of grown-in defects in the silicon. The image on the left also shows a high lifetime outer shell, a tell-tale sign of grown in defectactivation.