Australian National University

Public Dissemination Report

Heterocontact-Polysilicon Hybrid IBC Solar Cell (2020/RND013)

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1 Introduction

Interdigitated Back Contact (IBC) cell design represents among the most elegant device design for single-junction Si solar cell. Having both positive and negative contacts on the rear surface inherently simplifies opto-electrical trade-off considerations on the front surface by enabling unobstructed front light transmission for high photogeneration and minimal ohmic losses with wide rear metal fingers. This design technology has led the recent resurgence of Si efficiency records with a string of record-breaking devices.

Numerous Si single junction records were achieved using the IBC device design, where Panasonic's 25.6% SHJ IBC solar cell, breaking the long-standing 25.0% PERC cell record held since 1998. More recently, new records have been since been achieved, notably with the incorporation of hydrogenated amorphous silicon (a-Si:H) heterojunctions with an efficiency of 26.7% by Kaneka [1], and doped polysilicon technology via ion implantation demonstrated by ISFH with a 26.1% efficient device [2, 3].

ANU is among the small handful of institutes to have demonstrated IBC cell efficiencies of 25.0% and above, noting that the ANU results were achieved using conventional homojunction technology, and direct metal to doped Si contacts[4].

However, the key drawback in the technology is poor cost-performance ratio due to the complexity of forming the rear local contact diffusions and the interdigitated metal finger patterns [2, 3]. Addressing the need for a simplified fabrication sequence, this project proposes distinct innovative technological progressions by combining doped chemical vapour deposition (CVD) polysilicon tunnel-oxide (Poly-Si/Ox) passivated contacts with dopant-free carrier-selective contacts [5]. These technologies are investigated in parallel here to take advantage of its synergistic properties towards enabling elegant fabrication sequence and high-efficiency potential.

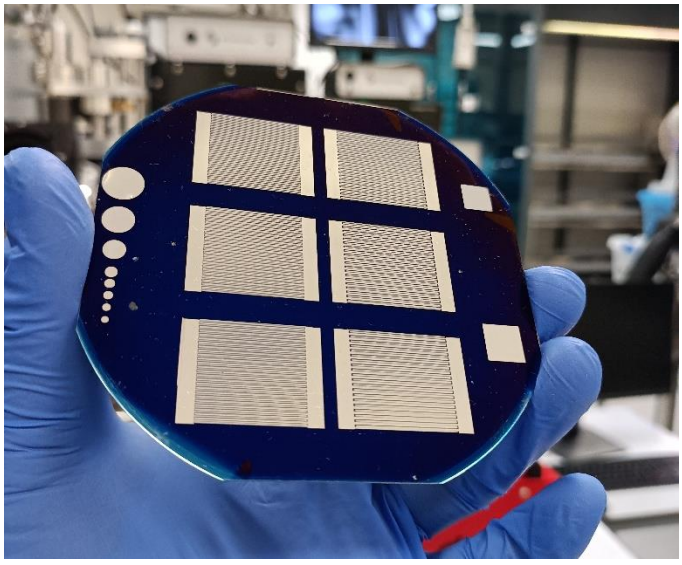

Figure 1: Laboratory scale IBC solar cells fabricated at ANU

2 Technical Details

2.1 Hybrid-IBC Si solar cell Design

This project proposes a revolutionary advancement in the IBC device design, through the inception of the Hybrid IBC Solar Cell design. This novel approach seeks to refine and enhance the IBC configuration by integrating state-of-the-art materials and fabrication techniques towards overcoming the inherit limitations of traditional IBC cells, particularly In terms of fabrication complexity and cost-efficiency. The core of this innovation takes advantage of the synergistic properties of incorporating polysilicon passivated contacts (PPC) and metal-oxide (MO) carrier selective contacts in a cell design. This proposed device features a PPC/MO recombination junction (RJ) as the minority carrier selective contact, and the MO contacts as the majority carrier contact. This combination is based on the unique advantages of each materials where PPC is known for its superior carrier collection capabilities and chemical resistance, and MO contacts are recognised for the low-temperature deposition, effectiveness as a selective carrier passivation, and ability to form the RJ when

deposited over a PPC layer. The combination of these properties offers specific advantages which significantly reduces fabrication complexity, while still enabling high efficiencies.

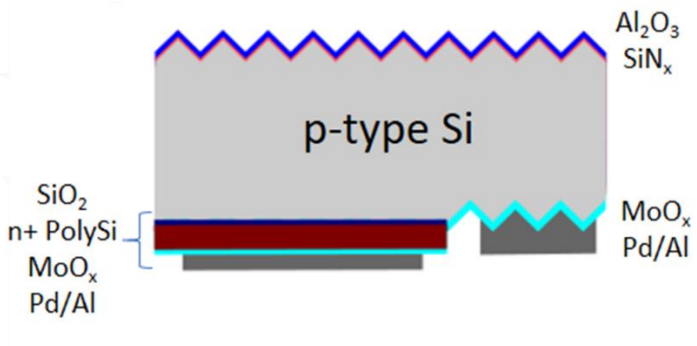

Figure 2: *Polysilicon-heterocontact hybrid IBC solar cell*

A cross sectional illustration of the proposed design is presented in Figure 2, which illustrates the unique approach to the IBC cell design. The front surface of the cell features a double-layer anti-reflection coating (ARC) typical of IBC cells, however the rear surface proposes a revolutionary change, which utilises a PPC/MO RJ as the device junction, and a MO contact as the majority carrier contact. The application of PPC as the junction formation layer enables formation of a highly ideal rectifying diode response, which is paramount in achieving high V_{OC} over 700mV and FF values exceeding 80%. Conversely the MO based carrier-selective layer used as the majority carrier contact allows development of a film that focuses on achieving carrier selectivity, excellent passivation and a low contact resistance.

The primary challenge in actualising a functioning prototype of this innovative device lies in the effectiveness of the PPC/MO RJ layer and the development of a fabrication sequence that facilitates its integration. This challenge is multifaceted, encompassing not only the material science behind the PPC/MO layer's properties, but also the engineering of a fabrication process that aligns with the nuanced requirements of these materials. A complete solution to this challenge would include development of the PPC/MO RJ layer, patterning techniques, compatible wet chemical processes for etching and texturing, and annealing that are compatible with the various materials. Additionally these processes must remain cost-effective or has the potential to be replaced with low-cost processes and become scalable to ensure that the design can be realised in large-scale manufacturing environments.

A solution to these challenges via the demonstration of a working prototype cell would validate the feasibility of the Hybrid IBC cell design, and unlocks new pathway for achieving higher efficiency while reducing manufacturing costs of IBC cell design.

2.2 Recombination Junction Development

Precursor to enabling the Hybrid-IBC cell concept, is the need for a recombination tunnel-junction contact consisting of a base n-type PPC, which can then be layered with capping metal-oxide layers of opposite polarity, towards enabling a self-aligning contact formation. Towards this goal, this project has successfully developed and demonstrated the functionality of a recombination tunnel junction based contact, consisting of n+ PPC capped with a MoO_x metal-oxide layer, forming a multi-functional stack consisting of MoO_x/n+ poly-Si/SiO_2/n+

Si/p-type Si bulk. This stack enables formation of the p-n junction, emitter layer, provides excellent passivation qualities, and low ohmic contact resistivity as the n-type contact. A transmission electron microscope (TEM) image is presented in Figure 1, showing the formed stack of layers going from the bulk Si wafer on the left to the metal contact side on the right.

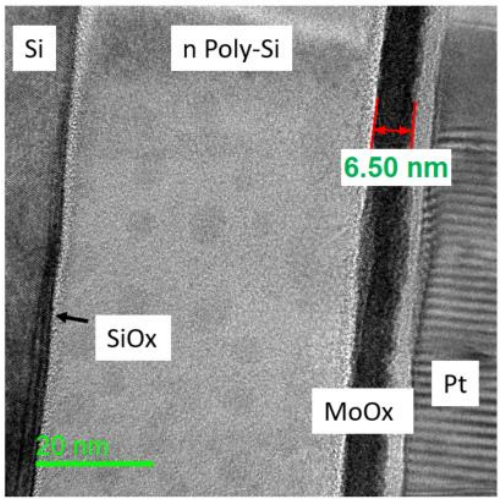

Figure 3: TEM image of a recombination junction stack consisting of MoO_x/n+ Poly-Si/SiO2/n+ Si/p-type Si bulk

The contact resistivity of this stack was characterised using the Cox and Strack method [6], with a structure featuring a range of metal contact dots of varying sizes, and a full rear metal contact. The cross-section graphical representation of this test structure is illustrated in Figure 2(left). The resulting analysis indicates that a relatively low resistivity of approximately 1 $m\Omega cm^2$ is attained with the proposed contact stack. This is consistent with high performance Si cell devices enabling > 25% cell efficiency. Importantly, the measurement of the contact resistance before and after MoO_x/Al deposition shows that the additional layers does not significantly affect the resistance loss through the stack, while still maintaining a highly ohmic contact behaviour as illustrated in Figure 2(right).

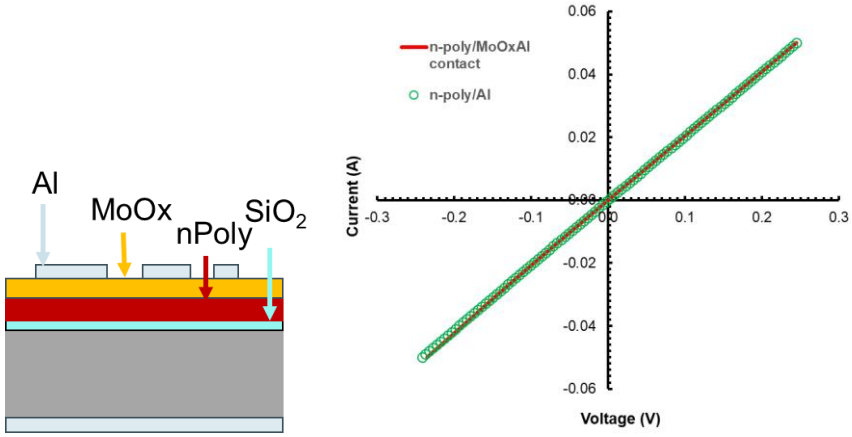

Figure 4: (left) Cross sectional illustration of the C&S cell structure, (right) I-V measurement of the an individual C&S contact dot showing highly ohmic characteristics before and after MoO_x/Al deposition

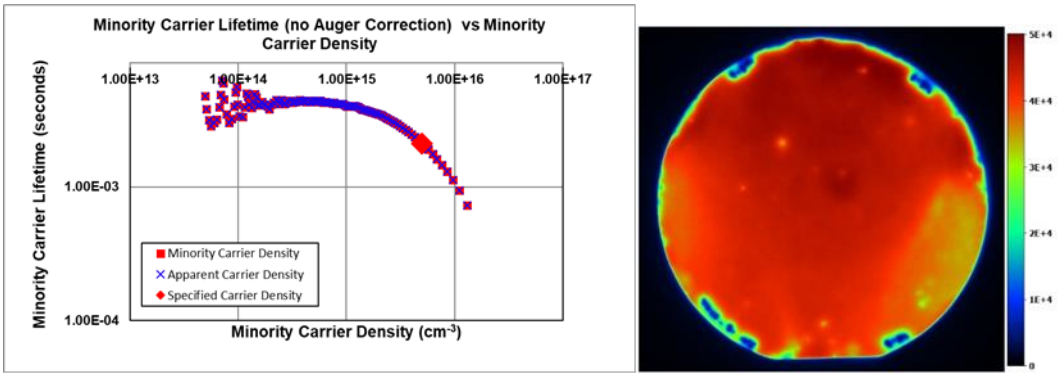

Figure 5: (left) PCD measurement of an n-type 2 Ωcm wafer with symmetrical passivation stack consisting of MoO_x/n+ poly-Si/SiO_2/n+ Si/p-type Si-bulk with lifetime over 2 ms at an injection level of 5 x 10^{15} cm^3, and (right) PL image of the test wafer showing excellent uniformity.

The surface passivation of this stack is characterised via Photoluminescence (PL) imaging, and Photoconductance Decay (PCD) measurements. The PCD measurements as presented in Figure 3(left) indicates high bulk lifetimes exceeding 2 ms and a J_0 value of below 7 $fAcm^{-2}$ which corresponds to an implied-V_{OC} of approximately 720 mV. The PL image of the test wafer is presented in Figure 3(right) which corroborates with the PCD measurement on its excellent surface passivation, while also demonstrating high level of uniformity, necessary for its application in larger cell wafers.

The characterisation of the surface passivation for this layered structure is conducted through PCD and PL measurements. The results derived from PCD as depicted in Figure 3(left) reveals effective lifetimes exceeding 2 ms, alongside an implied open-circuit voltage (V_{OC}) in the vicinity of 720mV, which correlates to a recombination current density (J_0) value of under 7 $fAcm^{-2}$. The PL image of the test structure is presented in Figure 3(right), which demonstrates a highly uniform passivation quality across the test wafer, a critical attribute for the effective implementation of this technology in larger scale solar cell wafers.

2.3 Prototype cell Fabrication

In this section, we will provide a detailed description of the cell fabrication process used towards the successful fabrication of the prototype cells. The fabrication procedure for the prototype devices is illustrated in Figure 4 in six key fabrication steps.

In **Step 1**, 2.6 Ω-cm float-zone (FZ) p-type wafers were prepared with an initial gettering process involving the use of phosphorus diffusion, followed by TMAH etching to getter and subsequently physically remove contaminants and impurities from the wafer. A thin oxide layer is grown thermally in a pure oxygen ambient at a temperature of 600°C for 5 minutes, which provides an ultra-thin layer of SiO_2 measuring approximately 1.2-1.5 nm. This thin layer of SiO_2 provides a barrier layer for electrical and dopant segregation, while also being sufficiently thin to enable carrier tunnelling and therefore electrical connectivity. The wafers are then coated with an intrinsic layer of polysilicon, deposited via low-pressure chemical vapour deposition (LPCVD) process at a temperature of 520 °C. Phosphorus dopants are then introduced via thermal diffusion, at an elevated temperature of between 800-900 °C using a $POCl_3$ source, which is then annealed at 900 °C to drive in the dopants through the polysilicon and tunnel oxide layers. A hydrogenating Silicon-Nitride layer was deposited which improves surface passivation and acts as a barrier layer for the subsequent patterning step.

In **Step 2**, a photolithographic process was used to expose the front and rear surface masking barrier, which enabled localised wafer texturing at intended regions.

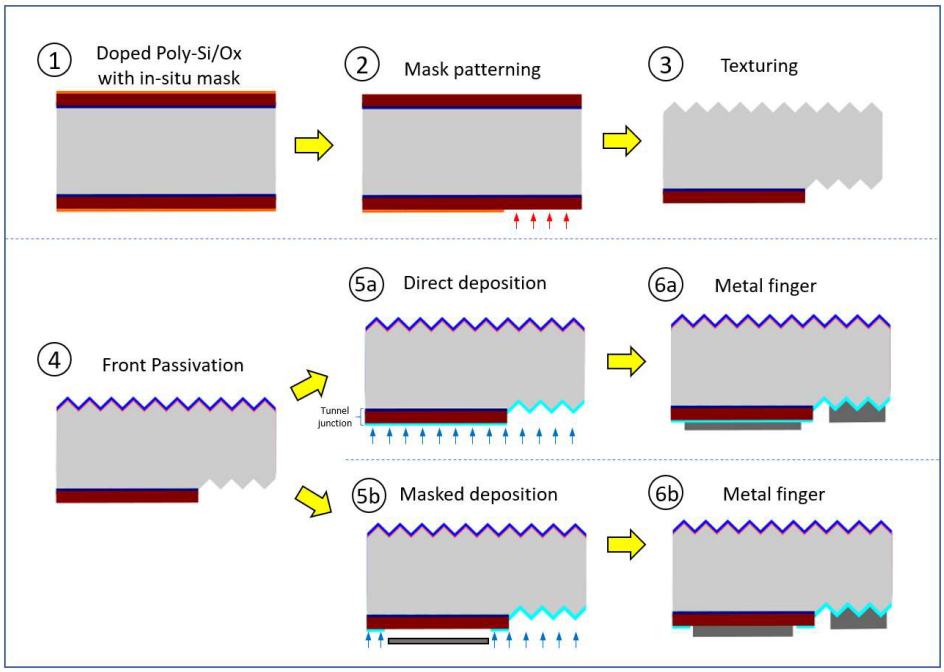

Figure 6: Fabrication process flow for the prototype Hybrid IBC solar cell. Details of each process step are as described in the text.

In **Step 3**, the wafers are textured in a KOH texturing solution. This process creates random pyramid textures, a key feature towards enabling high levels of light transmission into the solar cell. This texture-through-polysilicon process was successfully developed and trialled at ANU, which provides excellent random-texture uniformity, while maintaining localised coverage of doped polysilicon regions. A microscope image of the process is presented in Figure 5, with an inset figure showing the graphical illustration of the cross-sectional area of the local finger region.

In **Step 4**, surface passivation and anti-reflection coating consisting of Al_2O_3 and SiN_x. The Al_2O_3 is deposited via atomic-layer-deposition, while the Silicon-Nitride is deposited via PECVD. The PL imaging and the lifetime curve of the sample is presented in Figure 6, which indicates high uniform passivation, a high lifetime of 4.3 ms, and a low J_0 value of 4.3 fAcm^{-2}, corresponding to an implied-V_{OC} of over 730 mV on the p-type 2.6 Ωcm wafer.

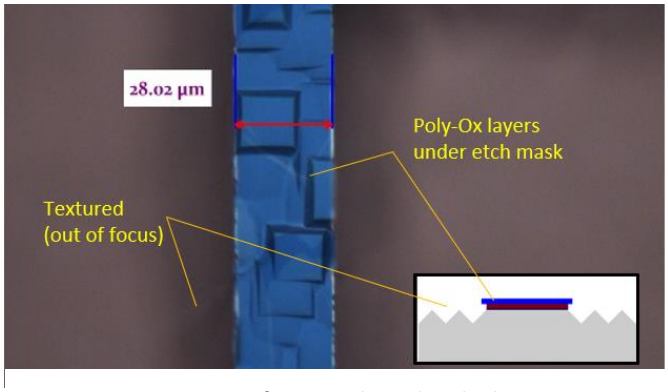

Figure 7: *Demonstration of texture-through-polysilicon process*

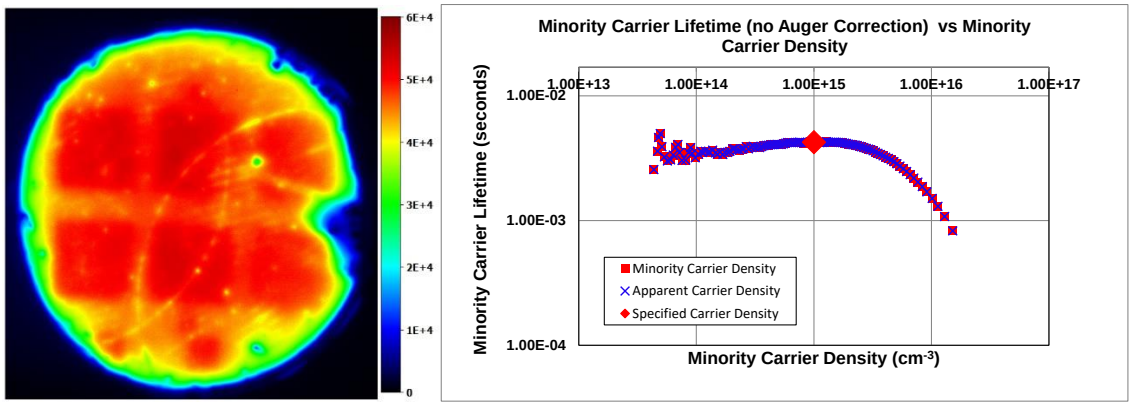

Figure 8: Surface passivation quality after dielectric layer passivation. (left) PL imaging demonstrating high lifetime and uniformity and (right) measured lifetime curve with an effective lifetime of 4.3ms at an injection level of 5 x 10^{15} cm^{-3}.

The prototype fabrication flow for the Hybrid IBC cells in this project follows the fabrication flow of **Step 5(a)** and **Step 6(a)** of Figure 4, where the MoO_x layer is deposited on the entire rear surface of the wafer without any shadow masking. In **Step 5(a)**, the entire rear surface of the wafer is coated with a 6.5nm thick layer of MoO_x, deposited via thermal evaporation from solid power source. This layer provides contact passivation, and carrier selectivity which provides a low resistive ohmic contact with approximately 1 Ωcm^2, as is elucidated in Section 1.1 of this report. Finally, in **Step 6**, metal contacting fingers are formed via deposition of aluminium via thermal evaporation through a shadow mask which simultaneously forms the n-type and p-type contacts, thereby completing the fabrication process.

2.4 Cell Results

This section will now present the outcomes and analytical assessments of the fabricated devices, focusing on the evaluation of the prototype cells' PL and I-V performance.

The fabricated Hybrid IBC cells are kept intact in the wafer for ease of measurement, and to minimise edge recombination losses from the cutting process to isolate each individual cell. This is shown in the photograph of a completed cell presented in Figure 8(right), where the six rectangular structures in the middle are the interdigitated rear finger structures of the prototype cells. The circles on the left and the square pads on the right are test structures for testing of contact resistivity and passivation quality respectively. The active area of the cell is 4 cm^2 (2 cm x 2 cm) and is defined by using an opaque aperture mask on the front surface during cell measurement.

The photoluminescence (PL) imaging of the cells and a top-down photo of the cell is presented in Figure 8 (left) and (mid) at two different stages of cell fabrication. Figure 8(left) provides the PL image immediately after surface passivation, while Figure 8(mid) is the PL image after metal contact formation is completed. The photograph of the cell, mirror-imaged to provide an identical orientation if presented in Figure 8 (right) for reference. The comparison between Figure 8 (left) and (right) provides an indication as to the passivation quality, and the recombination losses due to the metallisation process. The differing effects of metallisation on individual cells are due to a combination of having design variations in each cell (such as the contact opening sizes, cell finger pitch and spacing) as well as the natural variations in the process uniformity during fabrication.

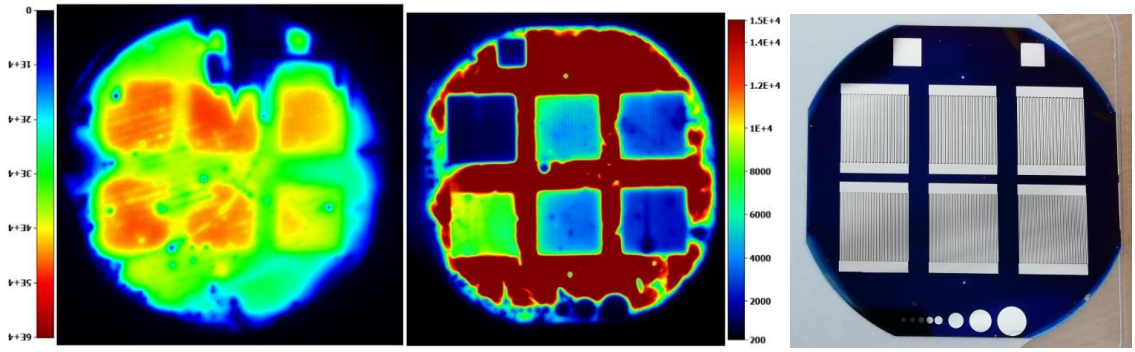

Figure 9: Photoluminascence images and Optical images of the final hybrid interdigitated Back Contact Solar Cells. (left) Photoluminance images of cells after Passivation, (mid) Photoluminance images following contact opening and final metallization where the active cell areas are the six square structures in each image, and (right) front images of the final IBC solar cells.

The solar cell parameters presented for the Hybrid-IBC technology are presented in Table 1, which provides a comprehensive set of performance metrics crucial for evaluating the efficiency of the cell. The open-circuit voltage (V_{OC}) of the champion cell was measured at 668 mV, indicating the maximum voltage the cell can produce when not connected to an external load. The short-circuit current density (J_{SC}) is recorded at 38.0 $mAcm^{-2}$, reflecting the current available from the cell under standard test conditions when the external circuit is shorted, essentially representing the cell's light-gathering capability. The fill factor (FF) is quantified as 0.55, indicating the cell's maximum power point is 55% of the theoretical maximum (V_{OC} x J_{SC}). Finally, the efficiency of the cell is measured to be 14.04%, which denotes the proportion of incident solar power that the cell converts to electrical energy under standard test conditions.

Table 1: Extracted cell characteristics from measured I-V data

	V_{OC}	J_{SC}	FF	η	FF_{pseudo}	η_{pseudo}	R_{series}	R_{shunt}
	mV	mAcm-2		%		%	Ωcm^2	Ωcm^2
Champion cell	668	38.0	0.55	14.04	0.73	18.48	5.1	375
Batch average	662	38.0	0.49	12.38	0.71	17.87	5.7	383

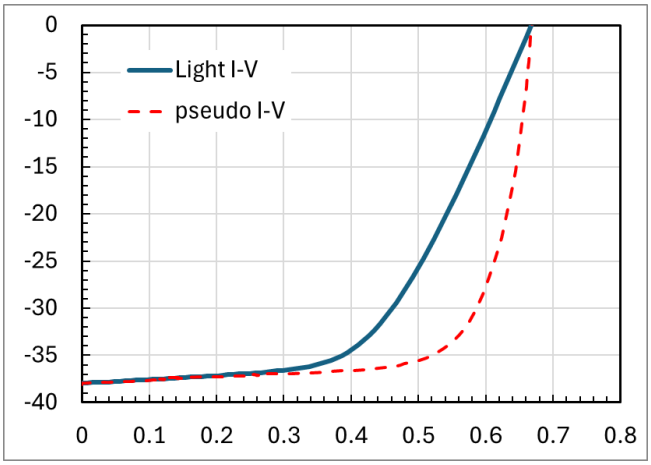

Figure 10: Light I-V and pseudo light I-V characteristics of the champion prototype cell.

The series resistance (R_{series}) of the cell as measured using the double-light method[7] is 5.1 Ωcm², which is a key factor in the measured final fill factor and overall efficiency of the prototype cells. Using the information from the R_{series} measurement, the pseudo fill factor (FF_{pseudo}) of the champion cell is analysed at 0.73, with a corresponding pseudo-efficiency of 18.48%, which represents the theoretical performance of the cell in the absence of series resistive losses.

The data for the batch average is relatively similar to the champion cell, albeit with poorer FF. This indicates good repeatability of the cell fabrication process, but also indicates specific fabrication defects that needs to be resolved to achieve higher device efficiency.

In conclusion, this section has showcased that each component's functionality within the technology was thoroughly verified through tests conducted on a working prototype which was fabricated using the proposed streamlined fabrication sequence.

3 Device Simulation and Technology Roadmap

This section explores the 3D simulation of the Hybrid IBC cell, which incorporates empirical data on its optical and electrical characteristics. The simulation aims to determine the highest possible efficiency of the cell design without manufacturing flaws, and its expected efficiency when scaled up to a larger surface area (over 100cm²). Additionally, comparing the simulation results with the prototype cell performance offers a method to quantify technological progress and highlights areas needing further improvements. This comparison enables us to develop a strategic roadmap of the cell performance towards a 25% device efficiency.

3.1 Simulation Parameters and Results

The simulation's input parameters come from test wafers processed in parallel with the cell's production wafers at every fabrication stage. These test wafers were periodically extracted and analysed using PCD (Photoconductive Decay) and PL (Photoluminescence) imaging. This analysis helps assess the passivation quality of the surface and the consistency of the process steps, providing critical insights into the electrical characteristics of the silicon wafer and the surfaces of the Hybrid IBC cell. The empirical data gathered, along with its area coverage within the cell design, is detailed in Table 2.

The optical properties of the device were measured via spectrophotometry, which enables analytical fitting of the device optics via ray-tracing optical models. Importantly, this by fitting the optical properties of the cell,

the 3D device simulation tools will be able to accurately recreate the photo-generation profile within the cell. The combined electrical and optical data provides the necessary inputs to perform a 3D device simulation. A 3D mesh of the simulation model is presented in Figure 9, showing the various active surface areas of the device.

Table 2: List of all active surface areas for the Hybrid IBC design, and empirically measured values for its electrical properties.

	Layer	Effective Area fraction	Electrical Properties
Front Surface	AlOx/SiNx	100% of front	6.2 fA cm^{-2}
Si Bulk	p-type Si	-	τ_{bulk} = 4.2 ms 2.6 Ωcm
n-type contact	Al/MoO_x/n+ Poly-Si/SiO_2/Si	50% (400/800 um)	6.25 fA cm^{-2} 25 mΩ cm^2
Rear passivated non-contact region	AlO_x/SiN_x	47.5% (380/800um)	5 fA cm^{-2}
p-type contact	Pd/MoO_x/Si	2.5% (20/800 um)	200 fA cm^{-2} 1 mΩ cm^2

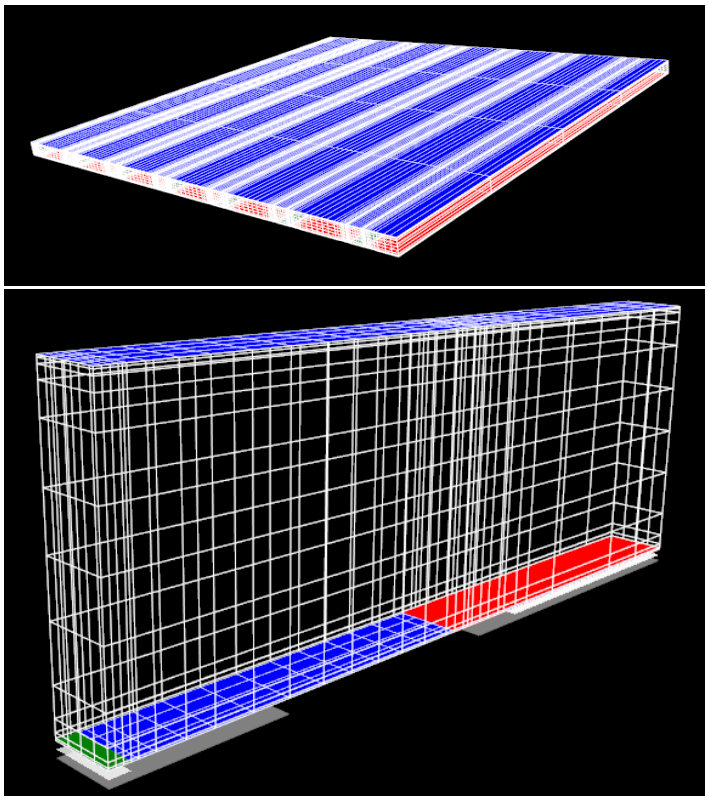

Figure 11: 3D mesh of the proposed Hybrid IBC cell design as generated using Quokka3 simulation tool showing (top) the mesh for a 10 x 10 cm or 100 cm^2 cell and (bottom) the mesh for an individual unit cell.

The simulations results from this model indicates that the proposed device design has a potential efficiency of 25%, with a J_{SC} of 41.6 $mAcm^{-2}$ and a V_{OC} of 723 mV with an active area of 10 x 10 cm. These values are consistent with the excellent passivation values obtained from the empirical measurements, and the high fill-factor is reflective of having optimised contact area for the respective contact resistivity on both the Poly/MoO_x n-contact and the MoO_x p-contact. The discrepancy to the prototype cell results of 18.5% are likely attributed to fabrication difficulties especially related to patterning steps, and will be discussed in detail in Section 3.2 on the roadmap towards 25%.

In order to understand the detailed loss analysis of the device, we utilise the Free Energy Loss Analysis (FELA) is presented in Figure 11, which provides a detailed breakdown of the cell losses from optical, ohmic, and recombination effects. The optical losses are typical for high efficiency IBC cells, consistent with losses from the 25% IBC cells at ANU in the past. The imperfect light trapping represents the difference between the measured cell optical performance as compared to the ideal lambertian light trapping with infinite cell thickness, noting that this is a highly hypothetical comparison. The reflection losses contribute to 0.39 $mWcm^{-2}$, and are typical for a AlO_x/SiN double-ARC front passivation layer on textured surface.

The recombination losses in the device are dominated by both the front and bulk recombination, with a recombination loss of 0.35 $mWcm^{-2}$ and 0.55 $mWcm^{-2}$ respective. Since IBC solar cells have both the n and p contact on the rear, the minority carrier pathway is significantly longer, resulting in increased sensitivity to front and bulk recombination effects.

The resistance losses of the cell is dominated by the hole and electron transport within the Si absorber bulk layer, which contributes to 0.19 $mWcm^{-2}$ and 0.38 $mWcm^{-2}$ respectively. The carrier transport power loss is related to the inherent design feature of IBC cells which has contacts on the rear. These losses are however compensated for the improved optical performance, as the cell is void of front finger shading losses typical to PERC and conventional front contact cell designs.

Importantly for this work, the p-type and n-type contact technologies developed in this project towards enabling the simplified hybrid IBC cell design is demonstrated to have a low contribution to the overall cell power loss. Specifically, the n+ poly-Si/MoO_x contact and non-contact recombination contributes to a power loss of 0.12 $mWcm^{-2}$, while the MoO_x contact contributes a total of 0.19 $mWcm^{-2}$. This is a significant outcome as it provides a demonstration of the potential for this technology to be applied in large area cells, while retaining it high efficiency potential.

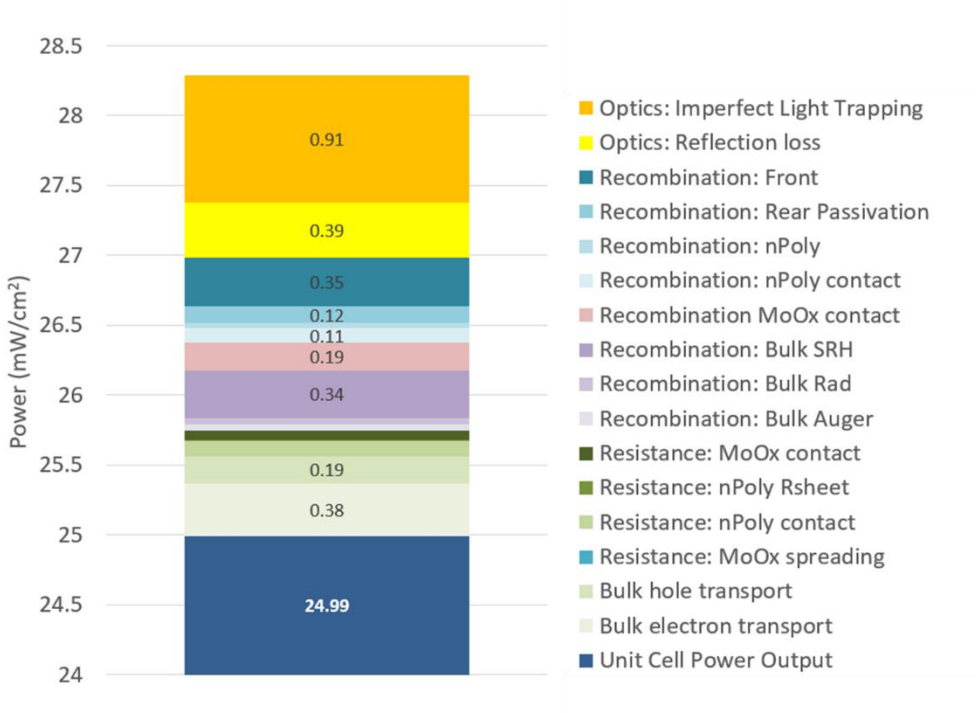

Figure 12: Free Energy Loss Analysis of the proposed Hybrid IBC design.

3.2 Technology Progression Roadmap towards 25% Efficiency

This section outlines the technological advancements and strategic steps required to achieve a 25% efficiency target in our prototype Hybrid Interdigitated Back Contact (IBC) Si solar cells. By analysing both empirical data and simulation results, we map a pathway to realize this efficiency milestone which is presented in Figure 12.

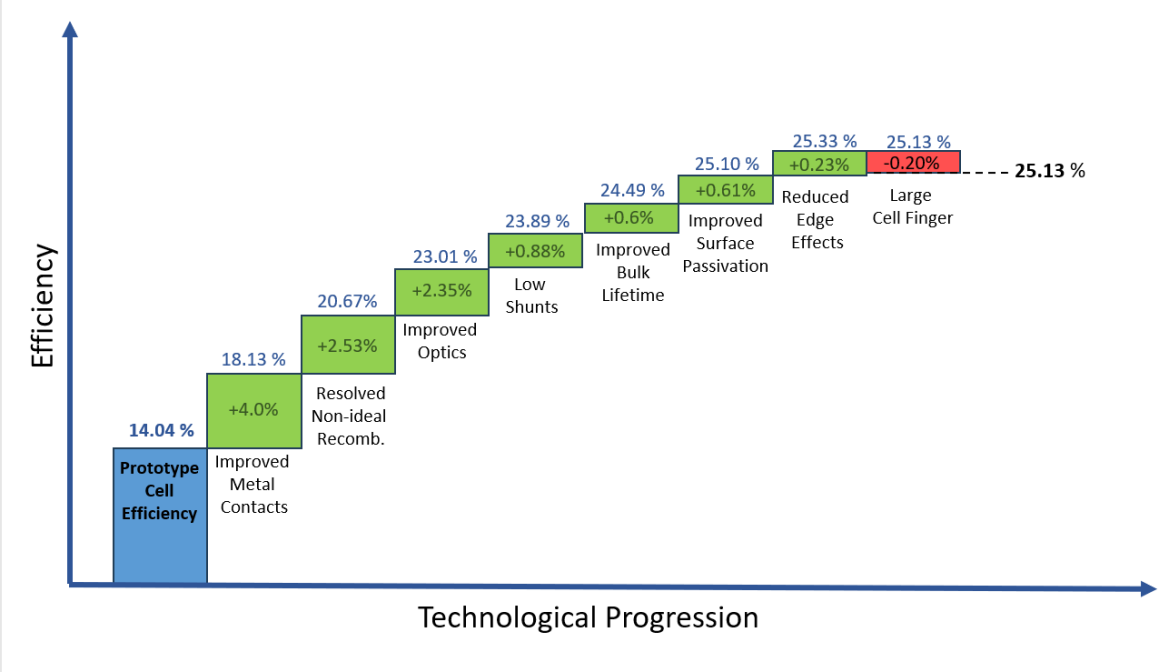

Figure 13: Roadmap of Technology Progression towards over 25% device efficiency

The presented roadmap outlines the incremental improvements required to achieve the targeted 25% efficiency, where each improvement addresses a specific limitation identified during the initial prototype fabrication and it quantified by its contribution to the final cell efficiency.

The initial performance of the prototype cell has demonstrated an efficiency of 14.1%. This serves as our baseline from which all improvements are measured.

- **Improved Metal Contact:** The champion prototype cell was measured to have high ohmic resistance losses, exceeding 5 Ωcm^2. This is higher industrial standards, and is likely due to the slow pace at which the device progress through the fabrication sequences which takes weeks rather than in a span of hours in an industrial setting. The amount of time elapsed between processing allows degradation of films due to oxidation and humidity. For instance, such effects were absent during contact tests demonstrated in Section 1.1 which indicates contact resistivity below 1 $m\Omega cm^2$ is expected in ideal fabrication conditions. The ability to replicate this process in an industrial setting is likely, and is expected to reduce contact resistivity of the device to below 100 $m\Omega cm^2$. This improvement is expected to improve cell efficiency by 4.0%, bringing the cell efficiency up to 18.13% which is corroborated with pseudo-FF results from the cell IV analysis.
- **Resolved non-ideal recombination:** The prototype cells demonstrated significant level of non-ideal recombination. Addressing this involves optimising the patterning process, particularly ensuring accurate alignment, and managing the doping profiles and junction depths along the boundaries of the doped polysilicon layer. Resolving non-ideal recombination will add another 2.53% to the cell efficiency.
- **Improved Optics:** The prototype cells had a simplified front optics, and measured a JSC of 38 mA/cm^2, which is significantly lower than the practical achievable limits of approximately 43.5 $mA\text{-}cm^2$.

Maximising the light trapping via double-anti reflection coating and improved front texturing processes is expected to improve the efficiency by another 2.35%.

- **Resolving Low Shunt Resistance:** The prototype cell had low shunt resistances, which causes low fill-factor and overall power losses within the cell. Improving alignment, and optimising isolating dielectric layers are expected to resolve this issue, and to improve the cell efficiency by 0.88%.
- **Improved Bulk lifetime:** Fitting of empirical data indicates that the prototype cell had a bulk lifetime of approximately 2.6 ms. This is causes significant losses to the fill factor, V_{OC}, and J_{SC} of the device. Utilisation of higher quality wafers, and optimising the process to include gettering process is likely to increase the bulk lifetime significantly towards approaching the Auger lifetimes. Successful implementation is expected to increase the efficiency by another 0.6%.
- **Improved Surface Passivation**: The prototype cell had a measured front surface passivation of 6.2 fA/cm^2 and a poly-Si/MoOx RJ non-contact J0 of 6.25 fA/cm^2. Towards higher device performance, further optimisation of front AlOx/SiNx surface passivation and the doped polysilicon layers can expect to reduce these value to approximately 1 fA/cm^2 consistent to current state of the art performances values. This improvement will potentially increase the cell efficiency by another 0.61%.
- **Reduced Edge Effects**: By minimising edge recombination via edge passivation techniques and with the move to larger cell sizes, we can add another 0.234% in efficiency.
- **Large cell finger resistances:** Transition of this cell design to industrial size wafers will likely increase the finger resistance of the device. This is expected to re-introduce some series resistance to the device, where an increase in approximately 0.1 Ωcm^2 is expected to reduce efficiency by 0.134%.

The combination of technological developments and improvements to the fabrication processes as outlined in this roadmap is expected to result in a final cell device efficiency of approximately 25.1%. This highlights the potential of the Hybrid-IBC cell design as a low-cost high-efficiency process.

4 Challenges and Pathways Towards Industrialisation

4.1 Polysilicon Patterning

The fabrication sequence proposed for the Hybrid IBC technology is notably streamlined, aligning well with high-volume manufacturing, with the notable exception being the polysilicon patterning step.

Polysilicon-passivated contacts offer several significant advantages over traditional contacts in silicon solar cells, especially in terms of providing superior surface passivation and facilitating a simplified fabrication process, akin to that employed in TOPCon solar cells. However, the challenge lies in the cost-effective patterning of the polysilicon layer for its viable integration into a manufacturing environment. While polysilicon patterning is feasible in laboratory settings and for prototype cell development, employing photolithography and etching for this purpose is considered economically impractical for large-scale production. Presently, there are several critical research avenues being explored in the area of polysilicon patterning.

Selective Doping and etching: This approach involves selectively doping the polysilicon layer only in areas where contacts are desired. This can be done via ink-jet printing, or laser defined masking steps. Once the selective doping is achieved, a selective etching process can be applied which preferentially etches only the undoped areas of the polysilicon, thereby leading to formation of localised doped polysilicon regions. This is a highly promising approach for its application to this cell technology in the future but is currently still under development and requires further research to achieve the desired level of control, contact quality, and process capability[8].

Laser doping and etching: A second approach is via utilisation of lasers which are capable of performing localised doping and localised etching of the polysilicon layer. A laser doping process typically involves

application of a dopant source layer, followed by application of laser pulses at designated areas to provide local doping. Laser based masking and etching can also be used to ablate and remove either the polysilicon layers directly, or to remove masking layers, after which the wafers can be etched to remove unwanted polysilicon regions. These process steps are highly promising and have been adopted for conventional cell fabrication, but the described techniques are yet to be successfully demonstrated for patterning of doped polysilicon structures such as TOPCon solar cells [9].

Patterning on polysilicon holds significant potential for high-efficiency silicon solar cells. However, overcoming the challenge of maintaining good passivation while achieving low-resistance contacts requires careful consideration of different approaches and ongoing research efforts. Recent advancements in buffer layer materials, deposition techniques, and metallization processes offer promising avenues for achieving this goal and paving the way for wider adoption of PPCs in the solar cell industry.

4.2 Scalability and Manufacturability of Metal-Oxide Tunnel Junctions

The development of metal-oxide tunnel junction layers, as presented in Section 1.1, has shown promising results in terms of passivation quality and low contact resistivity. However, the transition from laboratory-scale achievements to industrial-scale photovoltaic (PV) device production requires a detailed understanding and addressing of several key manufacturability aspects.

Firstly, it is critical in an industrial setting to achieve high consistency and quality control across multiple large batches of devices. For metal-oxide layers, this means ensuring uniform thickness and material composition. Although this high level of accuracy is demonstrated via a high-vacuum thermal evaporation process in the laboratory, it is a low-throughput and high-cost process which is impractical for up-scaling. The evaporation process should therefore be replaced with a higher throughput process such as the atomic-layer-deposition (ALD), which deposits via alternating between precursor gasses in a process which deposits single atomic layers of materials per cycle, in a highly controllable manner. Such processes have been demonstrated for the deposition of a wide range of metal oxides including the MoO_x demonstrated in this project.

The second consideration of the proposed technology is that it must be compatible with current PV cell manufacturing processes. Several adaptations to this technology will have to be developed which involves adapting the deposition to a high throughput process such as sputtering, Atmospheric Pressure CVD or ideally as discussed in the previous point, to utilise ALD for maximal deposition control. Furthermore, an efficient polysilicon patterning technology must also be developed as is discussed in Section 3.1. Once these challenges are overcome, the proposed fabrication sequence can be implemented using existing silicon cell production processes. The largest unknown cost of the final cell fabrication process will therefore depend heavily on the polysilicon patterning process which is currently yet to be determined, and is likely the biggest factor in the commercial viability of this technology.

Thirdly, we consider the durability and stability of the proposed technology. The recombination junction, and metal-oxide layers used must withstand a high-temperature fire-through contact formation processes, and be stable to environmental factors such as temperature fluctuations, humidity and UV exposure typical to outdoor settings. Long term stability tests, accelerated aging tests, and field trials will be necessary to validate the durability of these novel processes and materials. Progression of this technology will require strong industry partnership, industry funding and continual research collaborations with existing and possibly new partners towards adoption to pilot scale trials, module fabrication, and the subsequent outdoor testings.

5 Conclusion

This report comprehensively details the research activities executed to meet Milestone 3 of this project, highlighting the development and successful demonstration of the prototype Hybrid-IBC Si solar cell. This innovative prototype effectively integrates polysilicon passivated contacts (PPC) with metal-oxide based

contacts, simplifying the fabrication process by overcoming the challenges associated with advanced patterning and multiple doping phases.

A critical breakthrough was achieved with the development of the MoOx/n+ poly-Si recombination junction, which facilitated the creation of a high-performance p-n junction, serving as an effective emitter layer with excellent passivation and contact properties. The meticulous fabrication process, as detailed in Figure 4, which demonstrates the technical feasibility of the Hybrid-IBC cell but and provided a preliminary assessment of its scalability and potential integration into conventional manufacturing processes.

The empirical data-driven analytical assessments and 3D device simulations underscore the capability of large-area Hybrid-IBC cells to achieve efficiencies surpassing 24%. The roadmap to reaching and potentially exceeding a 25% efficiency threshold with the prototype cells is elaborated in Section 2, while Section 3 discusses the technological hurdles that must be overcome to ensure successful commercial adoption of this technology.

Publications to date

1) Tong, J., Le, T. T., Liang, W., Hossain, M. A., McIntosh, K. R., Narangari, P., . . . Fong, K. C. (2021). Impact of Pregrown SiOx on the Carrier Selectivity and Thermal Stability of Molybdenum-Oxide-Passivated Contact for Si Solar Cells. *ACS Applied Materials & Interfaces, 13*(30), 36426-36435. doi: 10.1021/acsami.1c06765
2) Liang, W., Narangari, P., Tong, J., Michel, J. I., Murdoch, B. J., Sio, H. C., . . . Fong, K. C. (2023). Effect of Al Electrodes on Surface Passivation of TiOx Selective Heterocontacts for Si Solar Cells. *physica status solidi (RRL) – Rapid Research Letters, 17*(3), 2200304. doi: https://doi.org/10.1002/pssr.202200304

References

[1] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano*, et al.*, "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%," *Nature Energy,* vol. 2, p. 17032, 2017.

[2] F. Haase, C. Hollemann, S. Schäfer, A. Merkle, M. Rienäcker, J. Krügener*, et al.*, "Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells," *Solar Energy Materials and Solar Cells,* vol. 186, pp. 184-193, 2018.

[3] C. Hollemann, F. Haase, S. Schäfer, J. Krügener, R. Brendel, and R. Peibst, "26.1%-efficient POLO-IBC cells: Quantification of electrical and optical loss mechanisms," *Progress in Photovoltaics: Research and Applications,* 2018.

[4] T. C. Kho, K. C. Fong, K. McIntosh, E. Franklin, M. Stocks, W. Liang*, et al.*, "Fabrication of 25.0% ONO IBC solar cell," in *SiliconPV 2019*, France, 2019.

[5] T. G. Allen, J. Bullock, X. Yang, A. Javey, and S. De Wolf, "Passivating contacts for crystalline silicon solar cells," *Nature Energy,* vol. 4, pp. 914-928, 2019/11/01 2019.

[6] R. H. Cox and H. Strack, "Ohmic contacts for GaAs devices," *Solid-State Electronics,* vol. 10, pp. 1213-1218, 1967.

[7] K. C. Fong, K. R. McIntosh, and A. W. Blakers, "Accurate series resistance measurement of solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 21, pp. 490-499, 2013.

[8] J. Wang, S. P. Phang, C. Samundsett, Z. Li, T. N. Truong, J. Yang*, et al.*, "Development of Phosphorus-Doped Nanoscale Poly-Si Passivating Contacts via Inkjet Printing for Application in Silicon Solar Cells," *ACS Applied Nano Materials,* vol. 6, pp. 140-147, 2023/01/13 2023.

[9] M. Vaqueiro-Contreras, B. Hallam, and C. Chan, "Review of Laser Doping and its Applications in Silicon Solar Cells," *IEEE Journal of Photovoltaics,* vol. 13, pp. 373-384, 2023.